Specificati n Amendments

Amend paragraph [0001] as follows:

[0001] This application is a continuation of application no. 10/278,551 filed October 22, 2002, which is a division of application no. 09/948,879 filed September 07, 2001, and is also related to co-pending ~~applications: Serial No._____, filed_____, entitled, "HIGH-VOLTAGE VERTICAL TRANSISTOR WITH A MULTI-LAYERED EXTENDED DRAIN STRUCTURE", and Serial No._____, filed_____, entitled, "HIGH-VOLTAGE LATERAL TRANSISTOR WITH A MULTI-LAYERED EXTENDED DRAIN STRUCTURE"~~ application no. 10/278,432 filed October 22, 2002, ~~both of~~ which applications are assigned to the assignee of the present application.

Amend paragraph [0009] as follows:

[0009] Although the device structures described above achieve high Vbd with relatively low on-state resistance as compared to earlier designs, there is still an unsatisfied need for a high-voltage transistor structure that can support still higher voltages while achieving a much lower on-state resistance.

Amend paragraph [0018] as follows:

[0018] A high-voltage field-effect transistor having an extended drain ~~or drift~~ region and a method for making the same is described. The HVFET has a low specific on-state resistance and supports high voltage in the off-state. In the following description, numerous specific details are set forth, such as material types, doping levels, structural features, processing steps, etc., in order to provide a thorough understanding of the present invention. Practitioners having ordinary skill in the semiconductor arts will understand that the invention may be practiced without many of these details. In other instances, well-known elements, techniques, and processing steps have not been described in detail to avoid obscuring the invention.

Amend paragraph [0021] as follows:

[0021] Source electrode 32 is electrically connected to N+ source regions 27, which are disposed in respective P-body regions 26. For example, N+ source region 27a is disposed in P-body region 26a; N+ region 27b is disposed in P-body region 27b, and so on. It is appreciated that a variety of alternative source electrode connections are also possible. The area of the P-body regions directly beneath gate 30 (between N+ source regions 27 and drift regions 22) comprises the IGFET channel region of the transistor. In this particular embodiment, the gate region is a metal-oxide semiconductor (MOS), and the IGFET is a NMOS transistor. Thus, the channel regions of HVFET 20 are defined at one end by N+ source regions 27 and at the other end by N-type drift regions 22, which extend vertically from gate oxide 29 down to the N+ substrate 21. Insulating layers 33 separate gate 30 from source electrode 32. <u>The drift regions define a path for current flow, herein referred to as the first direction.</u>

Amend paragraph [0022] as follows:

[0022] The n-type ~~extended drain or~~ drift regions 22 are separated laterally by insulating regions or dielectric layers 28. <u>This direction of separation is substantially orthogonal to the first direction and is herein referred to as the second direction.</u> In the embodiment of Figure 1, dielectric layers 28 extend vertically from beneath P-body regions 26 down to N+ substrate 21 along the full vertical length of the drift regions 22. By way of example, dielectric layers 28 may comprise silicon dioxide, but other insulating materials, such as silicon nitride, may also be used. Disposed within each of the dielectric layers 28, and fully insulated from the semiconductor substrate 21 and drift regions 22, is a field plate member 24. Field plate members 24 comprise a conducting layer of material such as heavily doped polysilicon, metal, metal alloys, etc. As shown in the embodiment of Figure 1, each of the field plate members 24 is electrically connected to source electrode 32. Alternatively, the field

plate members may be connected to a separate electrode. Gates 30 are also connected to a separate electrode (not shown). Drain electrode 31 provides electrical connection to the bottom of N+ substrate 21.

Amend paragraph [0023] as follows:

[0023] The extended drain region of vertical NMOS high-voltage transistor 20 of Figure 1 consists of a plurality of laterally interleaved layers of doped semiconductor material (e.g., n-type drift regions 22), insulating material (e.g., silicon dioxide dielectric layer 28), and conducting material (e.g., heavily-doped polysilicon). In the on state, a sufficient voltage is applied to the gate such that a channel of electrons is formed along the surface of the P-body regions 26. This provides a path in the first direction for electron current flow from source electrode 32, N+ source regions 27, through the channel regions formed in P-body regions 26, down through the N-type drift regions 22, through the N+ substrate 21, to drain electrode 31.

Amend paragraph [0026] as follows:

[0026] The thickness of both the N-type drift regions 22 and oxide layers 28 should be designed so as to guard against ~~prevent~~ premature avalanche breakdown. Avalanche breakdown can be avoided by making the drift region relatively narrow in the second direction, which reduces the ionization path and thereby increases the critical electric field at which avalanche occurs. In the same regard, making oxide layers 28 relatively wide in the second direction allows the device structure to support a larger voltage for a given critical electric field.

Amend paragraph [0056] as follows:

[0056] After formation of the N+ source region 105 an interlevel dielectric layer 106 [[if]] is formed over the device. In the embodiment of Figure 5, interlevel dielectric layer 106 comprises ordinary silicon dioxide that may be deposited and

patterned by conventional methods. Openings are formed in dielectric layer 106 and a conductive layer of material (e.g., metal, silicide, etc.) is deposited and patterned to produce the structure shown in Figure 5F. In this cross-sectional view, source electrode 109 provides electrical connection to N+ source region 105, and electrodes 110a and 110b provide electrical connection to field plate members 103a and 103b, respectively.

Amend paragraph [0064] as follows:

[0064] In the embodiment shown, a portion of dielectric layers [[112]] 102 isolates field plate members 103 from gate members 113. Alternatively, trenches 112 may expose the top portion of field plate 103 and the same processing steps used to create layers 116 may also be used to form dielectric layers on the sidewalls of the field plates to isolate the field plates from the gate members.